Low Power Low Voltage 4/5 Dual Modulus Prescaler using Hybrid Master Slave Flip-flop

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Abstract— The paper represents a 4/5 dual modulus prescaler circuit with use of hybrid master slave flip-flop and is simulated I 180n CMOS process technology. As a result, the average power consumption of the prescaler is 0.02mW and the propagation delay is of 12ns. The supply voltage of complete circuit is 0.9V and at 20 GHz Clock frequency. The new approach of our divided-by-4/5 dual modulus prescaler has been compared with other recent implementation showing that the proposed circuit successfully tradeoff between various parameters lke power and frequency.

Index Terms— Dual Modulus Prescaler, Frequency divider, Frequency synthesizer, Hybrid Master Slave Flip-flop, Low Voltage, Low power, Prescaler.

I. INTRODUCTION

The field of complementary metal–oxide–semiconductor (CMOS) integrated circuits has reached a level of maturity where it is now an obvious technology for higher scale integration, lower power consumption, and high-speed capability. These circuits are manufactured to achieve a high-speed prescaler. The speed of operation of prescalers is mainly limited by that of the divide-by-4/5 counter, which is the only partly operating at the maximum frequency. To take full advantage of the speed of such a prescaler, the DFF's and NAND gates among the synchronous counter have to be optimized together. Also, to operate at high speed, it is important to reduce the in effect capacitances of internal and external nodes, which ensures the decrease of the power consumption as well as of the propagation delay.

The high-speed frequency divider is a crucial block in frequency synthesizer for generating any range of frequencies from an oscillator used in wireless communications. Dual modulus prescalers are widely utilized in phase-locked frequency synthesizers to obtain programmable frequency division ratio. A dual-modulus prescaler generally comprises of a divide-by-N/N+1 unit and a number of asynchronous divide-by-2 units. The high-speed multi-GHz prescaler usually devours the largest share of power in the frequency synthesizer because the prescaler is usually executed with digital circuits with large power consumption at GHz range. Flip-flops and clock distribution network mostly account for 30–70% of the total chip power consumption [1, 2]. Flip-flops and latches are considered as indispensable components for design of synchronous digital VLSI systems. The highest operating frequency of clocked digital systems is determined by the flip-flops. The correct selection of flip-flop is done on the basis of factors like high performance, low power, transistor count, clock load, design robustness, power-delay, and power-area tradeoffs are generally well-thought-out before choosing a particular flip-flop design. Master-slave FFs are generally utilized for low power systems whereas other FF like pulse triggered FFs find their use in high speed applications.

II. HYBRID MASTER SLAVE FLIP-FLOP

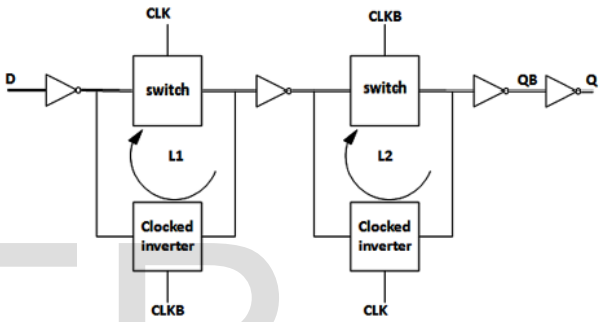

Fig.1. Conventional master-slave FF architecture

In the conventional master slave FF architecture as shown in figure 1, complementary outputs Q and QB are obtained by using two regenerative loops, L1, L2, one each in the master and the slave sections to maintain a static functionality. However, both the loops operate independently and become functional on complementary clock signals CLK and CLKB respectively. Regenerative loops generally require two cross coupled inverters.

In the traditional design technique, for each loop, one inversion takes place in the forward (critical) path while the other (clocked) inversion takes place in the feedback path and there is no shared component between both the loops.

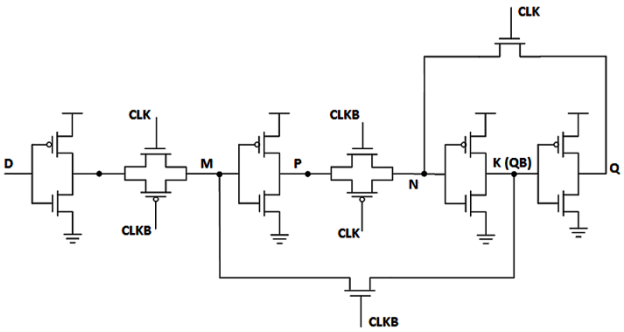

Fig. 2. Hybrid Master Slave Flip-flop

In Hybrid Master Slave Flip-flop (HMSFF) pass transistors are used which reduces the power dissipation. Hybrid maser slave flip-flop have high speed of operation as its important characteristic and have less capacitance of internal and external nodes, which leads to the reduction of power consumption as well as of the propagation delay. Consumed Average power is 0.02mW using 180nm. M and N nodes waveform is also shown showing the transitions at M and N node of master and slave flip-flop. From the given figure it is noticed that the inverted output of flip-flop that is QB is available at node K and further an inverter is added to get Q.

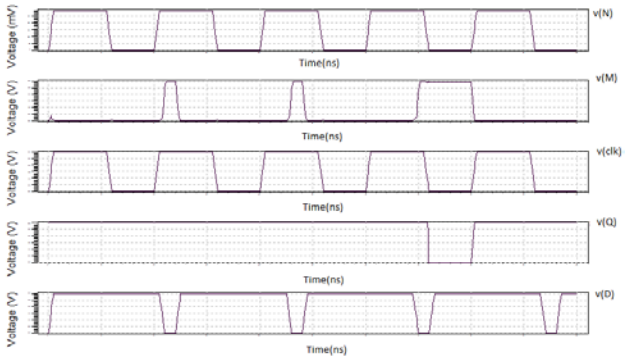

Fig. 3. Stimulations result of HMSFF

III. DUAL MODULUS DIVIDE- BY – 4/5 PRESCALER DESIGN

It consists of three DFF's, and several gates like NAND and NOR. The DFF's and the NAND and NOR gates form a synchronous divide-by-4/5 counter as shown in the figure3.

A conventional divide-by-4/5 prescaler is shown in Figure3: when mode signal M is high, the input signal *clock* traverses FF1 and FF2 and the circuit divides by four. When mode signal M is low, FF3 and the NOR-gate swallow one pulse every four input pulses and the circuit divides by five [3].

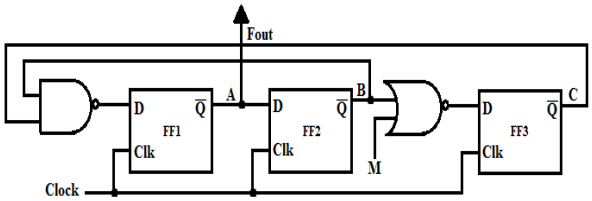

Fig.4. Conventional Divide-by-4/5 dual-modulus prescaler.

This synchronous counter creates the acute element for speed performance for higher divide N/N+1 counter, since it receives its clock signal with the maximum speed. The synchronous counter can be considered as a state machine with a transition state diagram like Fig. 5. The state machine input is the ***M*** signal, the output is signal ***A***, and the states are defined by the values of the signals ***A***, ***B***, and ***C***, the DFF outputs shown in Fig. 4. The synchronous operation is as follows: when the logical value at the ***M*** is HIGH, the circuit will go through the states 111, 101, 000 or 001, and 011, and the division by 4 is performed; when the logical value at the ***M*** is LOW, the circuit will go through the states 111, 101, 000 or 001,010, and 011, and the division by 5 is accomplished. The choice about counting up to 4 or 5 is done at the states 001 or 000 and, in consequence, these two states are the most critical in terms of timing [3].

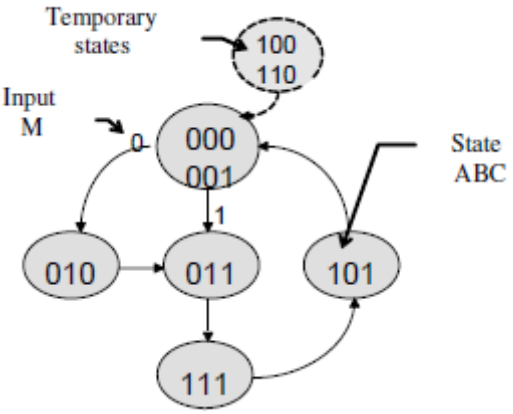

Fig.5. Transition state diagram of the Fig. 4 synchronous counter

The operating speed of prescalers is mainly limited by that of the divide-by-4/5 counter, which is the only partly operating at the maximum frequency. To maximize the speed of such a prescaler, the DFF's and NAND gates among the synchronous counter have to be optimized together. Also, to operate at high speed, it is important to reduce the effective capacitance of internal and external nodes, which leads to the reduction of the power consumption as well as of the propagation delay.

In this work Conventional D Flip-flop is switched by hybrid master slave which have high speed of operation as its important characteristic and have less capacitance at internal and external nodes, which leads to the reduced consumption of power as well as of the propagation delay. Schematic of the proposed design is given in figure 6.

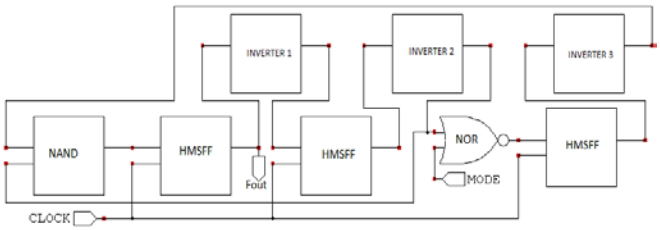

Fig.6: Proposed circuit of dual modulus prescaler using HMSFF.

IV. SIMULATION RESULTS

The proposed circuit of dual modulus prescaler 4/5 is implemented with other substitute prescalers to better evaluate the gains of hybrid master slave flip-flop. Keeping $W_{p,n} = 2L_{p,n}$.
Schematics are designed using schematics editor targeting 180nm technology. After simulation estimation of the average power consumed and propagation delay is implemented.

TABLE I. PERFORMANCE OF DIFFERENT PRESCALERS

Design parameters	Design [3]	Design [4]	Design [5]	Design [6]	Design [7]	This Work
Process(nm)	0.35	0.18	0.09	0.18	0.18	0.18
Voltage (V)	2.0	2.5	1.2	1.0	0.9	0.9
Max. Operating frequency(GHz)	1.61	9	44	6	18	20
Avg. Power (mW)	0.43	0.8	4.5	0.22	0.23	0.02

Table I illustrates the simulation performances of different prescalers and it is clearly visible that the results of proposed prescaler is much better than other prescaler.
Figure 7 illustrates the simulated waveforms for dual modulus prescaler for divide-by-5 in Fig. 7(a) when M=0 and divide-by-4 in Fig. 7(b) that is M=1 respectively.

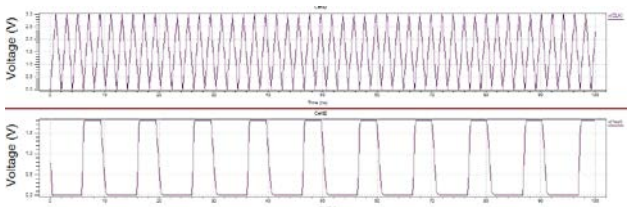

Fig. 7(a): Output Waveform of Dual modulus prescaler for mod 5.

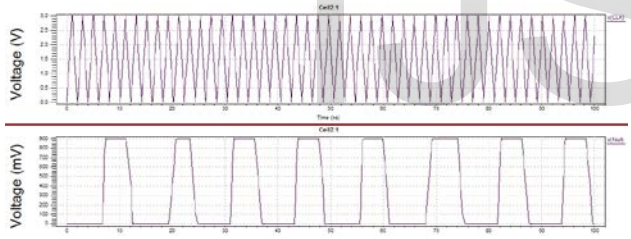

Fig. 7(b): Output Waveform of Dual modulus prescaler for mod 4.

It was observed that for the input of 20 GHz as a clock frequency the proposed dual modulus prescaler using hybrid master slave flip-flop was able to achieve frequency division of both mode 4 and mode 5 properly without huge noise problems.

V. CONCLUSION

In this work, the proposal of a high speed, low power consumption CMOS dual modulus prescaler is presented. The design and optimization of a hybrid master slave flip-flop based prescaler has been carried out by the analysis of the operating frequency and power consumption. An innovative divide by 4/5 unit with minimal power consumption has been offered. The experimental consequences of the proposed work associate very well when compared with other implementations. It is also observed that hybrid master slave flip-flop have high speed of operation as its important characteristic and have less capacitance of internal and external nodes, which leads to the reduction of power consumption as well as of the propagation delay. Therefore with the help of hybrid master slave flip-flop instead of conventional d flip-flop there was huge difference in power consumption was observed at 180nm technology with 0.9V at 20GHz clock frequency which is a quiet appreciable result.

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